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10/678,941	10/03/2003	Susumu Iwamoto	FUJI:205A	1192

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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,941	IWAMOTO ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/073,671.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figures 13 and 14 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 8-11 and 31-34 are objected to because of the following informalities: there is insufficient antecedent basis for "the surface". Appropriate correction is required.

Double Patenting

Claim 5 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 4. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 1, 2, 4-6, 8, 10, 12, 14, 16, 18, and 20 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-12 of prior U.S. Patent No. 6,674,126. This is a double patenting rejection.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 9 and 11 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 20 and 21 of U.S. Patent No. 6,674,126. Although the conflicting claims are not identical, they are not patentably distinct from each other

because if claim 9 were placed in independent form, it would be fully anticipated by claim 20 of US Pat. 6,674,126.

Claims 3, 7, 13, 15, 17, 19, 21-32, and 43-48 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 13 of U.S. Patent No. 6,674,126. Although the conflicting claims are not identical, they are not patentably distinct from each other because it is generally held that a broad/generic claim is obvious over a more narrow species claim. In this case, generic claims 3 and 24 are obvious over claim 13 (or claim 20) of US Pat. 6,674,126 and generic claim 22 is obvious over claim 1 of US Pat. 6,674,126.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 3, 7, 13, 15, 19, 24, 26, 30, 40, 42, 44, and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Tihanyi et al. (US Pat. 6,184,555, hereinafter Tihanyi).

In regards to claim 3 and 7, Figure 7d of Tihanyi discloses a semiconductor device comprising: a semiconductor chip having a first major surface (top) and a second major surface

(bottom) facing opposite to the first major surface; a first electrode layer 102 on the first major surface; an active region 98/99 in a vicinity of the first major surface, the active region being in electrical contact with the first electrode layer; a layer with a low electrical resistance 94 of a first conductivity type in the vicinity of the second major surface, a drain drift region between the first major surface and the layer with low electrical resistance, a third electrode layer (101 and 101') above the first major surface with an insulation film interposed therebetween, at least part of the third electrode layer being in close proximity to the first electrode layer; wherein the drain drift region comprises a first alternating conductivity type layer comprising vertically extending first semiconductor regions 95 of the first conductivity type and vertically extending. second semiconductor regions 96 of a second conductivity type arranged alternately at a first pitch of repeating; a breakdown withstanding region around the drain drift region, the breakdown withstanding region being between the first major surface and the layer with low electrical resistance, the breakdown withstanding region comprising a second alternating conductivity layer comprising vertically extending third semiconductor regions 95' of the first conductivity type and vertically extending fourth semiconductor regions 96' of the second conductivity type arranged alternately at a second pitch of repeating; an under region below the third electrode layer 101', the under region comprising a third alternating conductivity type layer comprising vertically extending fifth semiconductor regions 95' of the first conductivity type and vertically extending sixth semiconductor regions of the second conductivity type arranged alternately at a third pitch of repeating; and wherein the third arranged alternately arranged conductivity type layer is doped more lightly than the first alternating conductivity type layer. Note that is considered that second and third alternately conductivity type regions are one in the same. It is

inherent in a vertical MOSFET device that a second electrode layer (drain electrode) is provided on the second major surface. The device of Tihany is inherently capable of operating in the manner described by the following functional limitations: the drain drift region provides a vertical drift current path in the ON-state of the semiconductor device, the drain drift region being depleted in the OFF-state of the semiconductor device; the ON and OFF state of the semiconductor device is controlled through the third (gate) electrode; and the breakdown withstanding region provides substantially no current path in the ON-state of the device, the breakdown withstanding region being depleted in the OFF-state of the device.

In regards to claim 13, Figure 7d of Tihany discloses the first through sixth semiconductor regions of the first through third alternating conductivity type layers are shaped with respective stripes in a plane parallel to the first major surface.

In regards to claims 15 and 19, Figure 7d of Tihany discloses the pn-junctions in the second/third alternating conductivity type layer extend in parallel to the pn-junctions in the first alternating conductivity type layer.

In regards to claims 24 and 30, Figure 7d of Tihany discloses a semiconductor device comprising: a semiconductor chip having a first major surface (top) and a second major surface (bottom) facing opposite to the first major surface; a first electrode layer 102 on the first major surface having a first peripheral portion (portion above left side of electrode 101'); an active region 98/99 in a vicinity of the first major surface, the active region being in electrical contact with the first electrode layer; a layer with a low electrical resistance 94 of a first conductivity type in the vicinity of the second major surface, a drain drift region between the first major surface and the layer with low electrical resistance, wherein the drain drift region comprises a

first alternating conductivity type layer comprising vertically extending first semiconductor regions 95 of the first conductivity type and vertically extending second semiconductor regions 96 of a second conductivity type arranged alternately at a first pitch of repeating; a breakdown withstanding region around the drain drift region, the breakdown withstanding region being between the first major surface and the layer with low electrical resistance, the breakdown withstanding region comprising a second alternating conductivity layer comprising vertically extending third semiconductor regions 95' of the first conductivity type and vertically extending fourth semiconductor regions 96' of the second conductivity type arranged alternately at a second pitch of repeating; an under region below the first peripheral portion of the first electrode layer, the under region comprising a third alternating conductivity type layer comprising vertically extending fifth semiconductor regions 95' of the first conductivity type and vertically extending sixth semiconductor regions of the second conductivity type arranged alternately at a third pitch of repeating; and wherein the third arranged alternately arranged conductivity type layer is doped more lightly than the first alternating conductivity type layer. Note that is considered that second and third alternately conductivity type regions are one in the same. It is inherent in a vertical MOSFET device that a second electrode layer (drain electrode) is provided on the second major surface. The device of Tihany is inherently capable of operating in the manner described by the following functional limitations: the drain drift region provides a vertical drift current path in the ON-state of the semiconductor device, the drain drift region being depleted in the OFF-state of the semiconductor device; the ON and OFF state of the semiconductor device is controlled through the third (gate) electrode; and the breakdown

withstanding region provides substantially no current path in the ON-state of the device, the breakdown withstanding region being depleted in the OFF-state of the device.

In regards to claim 26, Figure 7d of Tihany discloses the first electrode layer 102 further comprises a second peripheral portion (portion above right side of electrode 101'), under which the second alternating conductivity type layer is extended.

In regards to claims 40 and 42, Figure 7d of Tihany discloses the first and second peripheral portions of the first electrode layer are formed on a thick insulation film (insulation film surrounding electrode 101').

In regards to claim 44, Figure 7d of Tihany discloses the first through sixth semiconductor regions of the first through third alternating conductivity type layers are shaped with respective stripes in a plane parallel to the first major surface.

In regards to claim 46, Figure 7d of Tihany discloses the pn-junctions in the second alternating conductivity type layer extend in parallel to the pn-junctions in the first alternating conductivity type layer.

Claims 3, 7, 9, 11, 13, 15, 17, 19, 21, 24, 26, 30, 32, 34, 36, 38, 44, 46, and 48 are rejected under 35 U.S.C. 102(e) as being anticipated by Minato et al. (US PGPUB 2003/0132450, hereinafter Minato).

In regards to claim 3, Figure 1 of Minato discloses a semiconductor device comprising: a semiconductor chip having a first major surface (top) and a second major surface (bottom) facing opposite to the first major surface; a first electrode layer 10 on the first major surface; a second electrode layer 11 on the second major surface; an active region 6/7 in a vicinity of the first

major surface, the active region being in electrical contact with the first electrode layer; a layer with a low electrical resistance 1 of a first conductivity type (n-type) in the vicinity of the second major surface, a drain drift region between the first major surface and the layer with low electrical resistance, a third electrode layer 9 above the first major surface with an insulation 8 film interposed therebetween, at least part of the third electrode layer being in close proximity to the first electrode layer; wherein the drain drift region comprises a first alternating conductivity type layer (center regions with most dense hatching) comprising vertically extending first semiconductor regions 3 of the first conductivity type and vertically extending second semiconductor regions 4 of a second conductivity type (p-type) arranged alternately at a first pitch of repeating; a breakdown withstanding region around the drain drift region, the breakdown withstanding region being between the first major surface and the layer with low electrical resistance, the breakdown withstanding region comprising a second alternating conductivity layer (regions with second most dense hatching) comprising vertically extending third semiconductor regions 3 of the first conductivity type and vertically extending fourth semiconductor regions 4 of the second conductivity type arranged alternately at a second pitch of repeating; an under region below the third electrode layer 9, the under region comprising a third alternating conductivity type layer (regions with least dense hatching) comprising vertically extending fifth semiconductor regions 3 of the first conductivity type and vertically extending sixth semiconductor regions 4 of the second conductivity type arranged alternately at a third pitch of repeating; and wherein the third arranged alternately arranged conductivity type layer is doped more lightly than the first alternating conductivity type layer (see paragraphs [0211] and [0214]) . The device of Tihany is inherently capable of operating in the manner described by the

following functional limitations: the drain drift region provides a vertical drift current path in the ON-state of the semiconductor device, the drain drift region being depleted in the OFF-state of the semiconductor device; the ON and OFF state of the semiconductor device is controlled through the third (gate) electrode; and the breakdown withstanding region provides substantially no current path in the ON-state of the device, the breakdown withstanding region being depleted in the OFF-state of the device.

In regards to claims 7 and 30, Figure 1 of Minato discloses the second alternating conductivity type layer is doped more lightly than the first alternating conductivity type layer (see paragraphs [0211] and [0214]).

In regards to claims 9 and 32, Figure 1 of Minato discloses a first well region 5 of the second conductivity type connected electrically to the first electrode layer 10, the first well region covering the surface of the third alternating conductivity type layer on the side of the first major surface.

In regards to claim 11, Figure 1 of Minato discloses the surface of the third alternating conductivity type layer on the side of the first major surface is in contact with the bottom of the first well region 5.

In regards to claims 13 and 44, Figure 1 of Minato discloses the first through sixth semiconductor regions of the first through third alternating conductivity type layers (3 and 4) are shaped with respective stripes in a plane parallel to the first major surface.

In regards to claims 15, 19, and 46, Figure 1 of Minato discloses the pn-junctions in the second/third alternating conductivity type layer extend in parallel to the pn-junctions in the first alternating conductivity type layer.

In regards to claims 17, 21, and 48, Figure 1 of Minato discloses the pn-junctions of the alternating conductivity type layers extend each extend in two directions: vertical and horizontal (up/down and into/out of the page). Therefore, it can be considered that the pn-junctions of the second/third alternating conductivity type layers extend in vertical direction (up/down) while the pn-junctions of the first alternating conductivity type layer extend in the horizontal direction (into/out of the page). Using this interpretation, Figure 1 of Minato discloses the pn-junctions in the second/third alternating conductivity type layers extend in perpendicular to the pn-junctions in the first alternating conductivity type layer.

In regards to claim 24, Figure 1 of Minato discloses a semiconductor device comprising: a semiconductor chip having a first major surface (top) and a second major surface (bottom) facing opposite to the first major surface; a first electrode layer 10 on the first major surface having a first peripheral portion (leftmost electrode 10); a second electrode layer 11 on the second major surface; an active region 6/7 in a vicinity of the first major surface, the active region being in electrical contact with the first electrode layer; a layer with a low electrical resistance 1 of a first conductivity type (n-type) in the vicinity of the second major surface, a drain drift region between the first major surface and the layer with low electrical resistance, wherein the drain drift region comprises a first alternating conductivity type layer (center regions with most dense hatching) comprising vertically extending first semiconductor regions 3 of the first conductivity type and vertically extending second semiconductor regions 4 of a second conductivity type (p-type) arranged alternately at a first pitch of repeating; a breakdown withstanding region around the drain drift region, the breakdown withstanding region being between the first major surface and the layer with low electrical resistance, the breakdown

withstanding region comprising a second alternating conductivity layer (regions with second most dense hatching) comprising vertically extending third semiconductor regions 3 of the first conductivity type and vertically extending fourth semiconductor regions 4 of the second conductivity type arranged alternately at a second pitch of repeating; an under region below the first peripheral portion, the under region comprising a third alternating conductivity type layer (regions with least dense hatching) comprising vertically extending fifth semiconductor regions 3 of the first conductivity type and vertically extending sixth semiconductor regions 4 of the second conductivity type arranged alternately at a third pitch of repeating; and wherein the third arranged alternately arranged conductivity type layer is doped more lightly than the first alternating conductivity type layer (see paragraphs [0211] and [0214]). The device of Tihany is inherently capable of operating in the manner described by the following functional limitations: the drain drift region provides a vertical drift current path in the ON-state of the semiconductor device; the drain drift region being depleted in the OFF-state of the semiconductor device; the breakdown withstanding region provides substantially no current path in the ON-state of the device; and the breakdown withstanding region being depleted in the OFF-state of the device.

In regards to claim 26, Figure 1 of Minato discloses the first electrode layer 10 further comprises a second peripheral portion (electrode 10 second from the left), under which the second alternating conductivity type layer is extended.

In regards to claim 34, Figure 1 of Minato discloses a second well region 5 (region 5 second from the left) of the second conductivity type connected electrically to the first electrode layer 10, the second well region covering the surface of the extended portion of the second alternating conductivity type layer on the side of the first major surface.

In regards to claim 36, as an alternative interpretation, the outside regions 3/4 (least dense hatching) can be the second alternating conductivity type layer and the middle regions 3/4 (regions with second most dense hatching) can be the third alternating conductivity type layer. Note that this interpretation is possible since both the second and the third alternating conductivity type layers are doped more lightly than the first alternating conductivity type layer. Also, the first and second wells can be switched, meaning the well region 5 second from the left is the first well region. Therefore, Figure 1 of Minato discloses the outermost second semiconductor region 4 of the first alternating conductivity type layer in contact with the innermost fifth semiconductor region 3 of the third alternating conductivity type layer is connected to the first well region 5 of the second conductivity type.

In regards to claim 38, Figure 1 of Minato discloses the outermost second semiconductor region 4 of the first alternating conductivity type layer in contact with the innermost third semiconductor region 3 of the second alternating conductivity type layer is connected to the second well region 5 of the second conductivity type.

Allowable Subject Matter

Claims 33, 35, and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Matthew C. Landau

Examiner

September 17, 2004